

Midterm 2 Preparation

CS 3853 Computer Architecture, Spring 2024

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Goals and Topics

- ▶ The goal is to help you systematically review the basic knowledge in Computer Architecture.
 - Only basic knowledge is tested.
 - No trick questions.
- ▶ Topics for this exam:
 - Basic CPU Implementation
 - Pipelining
 - Speculative Execution (branch prediction)

Location, Time and Logistics

- ▶ March 27th 2024, Wednesday, in-class, through Canvas
- ▶ Close-book, close-notes, close everything
- ▶ You can bring a calculator, but no cellphones.
 - The math is simple, you probably won't need a calculator.
- ▶ Do not waste time – if you stuck on a problem, move forward and revisit the problem later.
- ▶ The exam have Conceptual questions and Problems.
 - The problems will be similar as those in assignment 3.
- ▶ Don't leave a question empty. There is no penalty for wrong answers.
- ▶ You need to show your work and provide justifications with math computations/equations.

Materials to Review

- ▶ Slides, all questions are from slides
 - Make sure to always get the latest slides from Blackboard. I will update them to fix errors.
- ▶ Assignment 3.
- ▶ You can check out the textbooks, but it is not required.
 - There are some differences in the details between my slides and the textbooks. Please follow my slides in those cases.

Basic CPU Implementation

- ▶ Know the five stages of basic RISC and know what does each stage do.
 - IF, ID, EX, MEM and WB.
 - In particular, ID, EX, and MEM each has more than one operations.
- ▶ Understand the multiplexer.
 - A multiplexer is a device that selects one of several inputs.
 - A multiplexer is controlled by the control signal.
 - Know where the multiplexers are used in CPU, e.g., the selection of source operands for the ALU.
- ▶ Clock signals: edges, read and write at different edges.
- ▶ The data paths for three types of instructions: ALU, memory and branch instructions.

Basic CPU Implementation cont'd

- ▶ The CPU components/functional units used in each stage of execution.
 - There are questions about these components and their connections.
- ▶ Multi-cycle CPU design.
 - The benefits of multi-cycle CPU design.
- ▶ Exceptions
 - The definition of exceptions and interrupts.
 - The Control (unit) is responsible for handling exceptions.
And how?

Pipelining

- ▶ Know the solutions to all types of hazards
 - Slide 37 has a summary of these solutions.
 - You also need to know whether a solution can properly solve the hazards or not. In particular,
 - ▶ Why only branch prediction is the only practical solution to control hazard? Why other solutions do not work well?
 - ▶ Does data bypassing/forwarding eliminate stalls? And why?
 - ▶ How does reordering eliminate the stall from load-use?
- ▶ The definition superscalar CPUs.
- ▶ At least one problem about pipelining. The problem is similar to those in assignment 3.
 - In particular, you need to know how the pipeline works when stalling is the only solution to the hazards.

Branch Prediction

- ▶ Two-bit saturating counter for branch prediction.
 - You need to memorize the state machine.
- ▶ Know the implementation of Branch Prediction Buffer and Branch Target Buffer.
 - What components do these two buffers have?
 - How does a branch locate its entries in these two buffers?
- ▶ Correlating branch prediction
 - When does correlating branch prediction work?
 - When does correlating branch prediction fail to work?
 - The implementation of correlating branch prediction with Global Branch History Register (GBHR) and two-bit saturate counters.
- ▶ There will be one problem about branch prediction, similar to the last question of Assignment 3.